Abstract of the Disclosure:

A first and a second memory circuit are tested in parallel. It is possible to activate the memory circuits depending on a circuit select signal, and it is possible to apply a control signal to the first and second memory circuits. The control signal initiates a function in the respective memory circuit depending on the activation of the first or second memory circuit. In testing the memory circuits, the circuit select signal is applied to the first memory circuit and the inverted circuit select signal is applied to the second memory circuit, so that the function is initiated in the first or in the second memory circuit depending on the circuit select signal.

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